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Terms	Documents
((virtual or logical) near5 port) same concentrator	31

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<u>L3</u>	((virtual or logical) near5 port) same concentrator	31	<u>L3</u>
<u>L2</u>	((virtual or logical) near5 port) same concentrator same bus	1	<u>L2</u>
<u>L1</u>	((virtual or logical) near5 port) same physical same concentrator same bus	1	<u>L1</u>

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((virtual or logical) near5 port) same concentrator	1

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L4 ((virtual or logical) near5 port) same concentrator

1 L4

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L3 ((virtual or logical) near5 port) same concentrator

31 L3

L2 ((virtual or logical) near5 port) same concentrator same bus

1 L2

L1 ((virtual or logical) near5 port) same physical same concentrator same bus

1 L1

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L1 and concentrator	0

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<u>L4</u>	L1 and concentrator	0		<u>L4</u>
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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

<u>L3</u>	L1 same concentrator	1		<u>L3</u>
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<u>L2</u>	L1 and concentrator	36		<u>L2</u>
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<u>L1</u>	((virtual or logical) near10 port) same bus	1197		<u>L1</u>
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Term:	<div style="border: 1px solid black; padding: 2px;"> L1 and concentrator <div style="text-align: right;"> <div style="border: 1px solid black; width: 20px; height: 15px; margin-bottom: 2px;"></div> <div style="border: 1px solid black; width: 20px; height: 15px;"></div> </div> </div>
Display:	<div style="border: 1px solid black; padding: 2px; display: inline-block;">10</div> Documents in Display Format: <div style="border: 1px solid black; padding: 2px; display: inline-block;">-</div> Starting with Number <div style="border: 1px solid black; padding: 2px; display: inline-block;">1</div>
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<u>L3</u> L1 same concentrator	1	<u>L3</u>
<u>L2</u> L1 and concentrator	36	<u>L2</u>
<u>L1</u> ((virtual or logical) near10 port) same bus	1197	<u>L1</u>

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IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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1. A multiprocessor architecture for high-rate communication processing

Johnson, E.E.;

Military Communications Conference, 1991. MILCOM '91, Conference Record, 'Military Communications in a Changing World', IEEE

4-7 Nov. 1991 Page(s):1001 - 1006 vol.3

Digital Object Identifier 10.1109/MILCOM.1991.258421

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2. Evaluation of Futurebus+ for a GMMP multiprocessor

Johnson, E.E.; Moore, R.S.; Polson, J.T.;

Computing and Information, 1992. Proceedings. ICCI '92., Fourth International Conference on 28-30 May 1992 Page(s):441 - 444

Digital Object Identifier 10.1109/ICCI.1992.227617

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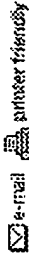
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A multiprocessor architecture for high-rate communication processing

Johnson, E.E.
New Mexico State Univ., Las Cruces, NM, USA;

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Abstract

The author presents a general-purpose multiprocessor architecture which accommodates an I/O bandwidth of many Gb/s through the use of VRAM in the main memory. The **virtual port** memory architecture is a global-memory-message-passing multiprocessor which is well suited to I/O-intensive real-time processing. This **bus-based** architecture permits incremental adjustments in I/O bandwidth, memory size, and processing power by simply adding or removing I/O controllers, memory modules, and processors. This architecture is described, followed by an analysis of its performance in handling various communication processing tasks, including the 4x300 Mb/s data stream at the NASA Tracking and Data Relay Satellite System (TDRSS) ground terminal

Index Terms

Inspe

Controlled Indexing

computer networks data communication systems multiprocessor systems parallel architectures satellite relay systems telecommunications computing

Non-controlled Indexing

NASA Tracking and Data Relay Satellite System VRAM bus-based architecture data communication global memory-message-passing multiprocessor high-rate communication processing multiprocessor architecture performance virtual port memory architecture

Author Keywords

Not Available

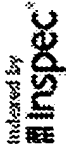
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